

WHAT IS CLAIMED IS:

1 1. A differential difference amplifier for amplifying an
2 input signal close to a negative supply voltage and adding an
3 offset voltage to the amplified input signal, said differential
4 difference amplifier comprising:

5 a first non-inverting input terminal capable of being
6 coupled to said input signal;

7 a first inverting input terminal capable of being
8 coupled to said negative supply voltage;

9 a second inverting input terminal capable of being
10 coupled to a feedback resistor coupled to an output of said
11 differential difference amplifier;

12 a second non-inverting input terminal capable of being
13 coupled to said offset voltage;

14 a first differential transistor pair comprising a first
15 transistor having a gate coupled to said first non-inverting
16 input and a second transistor having a gate coupled to said
17 first inverting input;

18 a second differential transistor pair comprising a
19 third transistor having a gate coupled to said second non-
20 inverting input and fourth transistor having a gate coupled to

21 said second inverting input;

22 a first cascode transistor pair comprising a fifth
23 transistor having a gate coupled to said first non-inverting
24 input and a source coupled to a drain of said first transistor
25 and a sixth transistor having a gate coupled to said first
26 inverting input and a source coupled to a drain of said second
27 transistor; and

28 a second cascode transistor pair comprising a seventh
29 transistor having a gate coupled to said second non-inverting
30 input and a source coupled to a drain of said third transistor
31 and an eighth transistor having a gate coupled to said second
32 inverting input and a source coupled to a drain of said fourth
33 transistor.

1 2. The differential difference amplifier as set forth in
2 Claim 1 wherein a source of said first transistor and a source
3 of said second transistor are coupled to the output of a first
4 bias current generating source.

1 3. The differential difference amplifier as set forth in
2 Claim 2 wherein a bulk connection of said first transistor and
3 a bulk connection of said second transistor are coupled to said
4 offset voltage.

1 4. The differential difference amplifier as set forth in
2 Claim 3 wherein a bulk connection of said fifth transistor and
3 a bulk connection of said sixth transistor are coupled to said
4 sources of said first and second transistors.

1 5. The differential difference amplifier as set forth in
2 Claim 4 wherein a source of said third transistor and a source
3 of said fourth transistor are coupled to the output of a second
4 bias current generating source.

1 6. The differential difference amplifier as set forth in
2 Claim 5 wherein a bulk connection of said third transistor and
3 a bulk connection of said fourth transistor are coupled to a
4 positive supply voltage.

1 7. The differential difference amplifier as set forth in
2 Claim 6 wherein a bulk connection of said seventh transistor and
3 a bulk connection of said eighth transistor are coupled to said
4 sources of said third and fourth transistors.

1 8. The differential difference amplifier as set forth in
2 Claim 7 wherein a drain current of said fifth transistor and a
3 drain current of said seventh transistor are combined to produce
4 a first composite current.

1 9. The differential difference amplifier as set forth in
2 Claim 8 wherein a drain current of said sixth transistor and a
3 drain current of said eighth transistor are combined to produce
4 a second composite current.

1 10. The differential difference amplifier as set forth in
2 Claim 9 further comprising a current difference detection
3 circuit capable of detecting a current difference in said second
4 and first composite currents and generating an output voltage
5 proportional to said current difference.

1 11. A battery monitoring apparatus comprising:

2 a sense resistor coupled to a battery such that a
3 charge current flows through said sense resistor when said
4 battery is charging and a discharge current flows through said
5 sense resistor when said battery is discharging;

6 an offset voltage generation circuit capable of
7 generating an offset voltage;

8 a differential difference amplifier for amplifying a
9 voltage sense signal on said sense resistor and adding said
10 offset voltage to the amplified voltage sense signal, said
11 differential difference amplifier comprising:

12 a first non-inverting input terminal capable of
13 being coupled to said voltage sense signal;

14 a first inverting input terminal capable of being
15 coupled to a negative supply voltage;

16 a second inverting input terminal capable of being
17 coupled to a feedback resistor coupled to an output of said
18 differential difference amplifier;

19 a second non-inverting input terminal capable of
20 being coupled to said offset voltage;

21 a first differential transistor pair comprising a

22 first transistor having a gate coupled to said first non-
23 inverting input and a second transistor having a gate
24 coupled to said first inverting input;

25 a second differential transistor pair comprising
26 a third transistor having a gate coupled to said second
27 non-inverting input and fourth transistor having a gate
28 coupled to said second inverting input;

29 a first cascode transistor pair comprising a fifth
30 transistor having a gate coupled to said first non-
31 inverting input and a source coupled to a drain of said
32 first transistor and a sixth transistor having a gate
33 coupled to said first inverting input and a source coupled
34 to a drain of said second transistor; and

35 a second cascode transistor pair comprising a
36 seventh transistor having a gate coupled to said second
37 non-inverting input and a source coupled to a drain of said
38 third transistor and an eighth transistor having a gate
39 coupled to said second inverting input and a source coupled
40 to a drain of said fourth transistor; and

41 an analog-to-digital converter ADC coupled to an output
42 of said differential difference amplifier for converting said

43 amplified voltage sense signal and said offset signal to a
44 digital signal readable by a processing circuit couple to said
45 ADC.

1 12. The battery monitoring apparatus as set forth in
2 Claim 11 wherein a source of said first transistor and a source
3 of said second transistor are coupled to the output of a first
4 bias current generating source.

1 13. The battery monitoring apparatus as set forth in
2 Claim 12 wherein a bulk connection of said first transistor and
3 a bulk connection of said second transistor are coupled to said
4 offset voltage.

1 14. The battery monitoring apparatus as set forth in
2 Claim 13 wherein a bulk connection of said fifth transistor and
3 a bulk connection of said sixth transistor are coupled to said
4 sources of said first and second transistors.

1 15. The battery monitoring apparatus as set forth in
2 Claim 14 wherein a source of said third transistor and a source
3 of said fourth transistor are coupled to the output of a second
4 bias current generating source.

1 16. The battery monitoring apparatus as set forth in
2 Claim 15 wherein a bulk connection of said third transistor and
3 a bulk connection of said fourth transistor are coupled to a
4 positive supply voltage.

1 17. The battery monitoring apparatus as set forth in
2 Claim 16 wherein a bulk connection of said seventh transistor
3 and a bulk connection of said eighth transistor are coupled to
4 said sources of said third and fourth transistors.

1 18. The battery monitoring apparatus as set forth in
2 Claim 17 wherein a drain current of said fifth transistor and a
3 drain current of said seventh transistor are combined to produce
4 a first composite current.

1 19. The battery monitoring apparatus as set forth in
2 Claim 18 wherein a drain current of said sixth transistor and a
3 drain current of said eighth transistor are combined to produce
4 a second composite current.

1 20. The battery monitoring apparatus as set forth in
2 Claim 19 further comprising a current difference detection
3 circuit capable of detecting a current difference in said second
4 and first composite currents and generating an output voltage
5 proportional to said current difference.